REMARKS

Applicant requests that the Examiner consider the references listed on the PTO-1449 forms submitted with the Information Disclosure Statements filed on December 30, 1999 and January 22, 2002 and initial same, thereby confirming that the listed references have been considered.

Applicant herein amends claims 1-15 and 17-30 to remove the phrase "integrated circuit" from the preamble of the claims. This amendment was not done for reasons of patentability, and does not narrow the literal scope of the preamble of claims 1-15 and 17-30.

Claims 1-15 and 17-30 are all the claims presently pending in the application.

1. In the Office Action dated May 6, 2002, the Examiner again requests that Applicant furnish drawings to facilitate the understanding of the invention, in compliance with 37 C.F.R. § 1.81. Contrary to the Examiner's statement, Applicant has furnished drawings (see above) that are in compliance with 35 U.S.C. § 113 and 37 C.F.R. § 1.81, and that do provide an understanding of the invention. In the Submission of Formal Drawings filed on July 2, 2002 (copy attached hereto), Applicant explained at length how the drawings correspond to the claims. The Examiner is obligated to provide specific evidence that the claimed elements are not showing in the Formal Drawings. *See In re Zurko*, 258 F.3d 1379, 1386 (Fed. Cir. 2001). The Examiner has not provided any concrete evidence, other than her unsupported statements, that the Formal Drawings do not show the claimed elements. Thus, Applicant believes that any corrections or revisions to the Formal Drawings are unnecessary.

Applicant's undersigned representative has attempted to arrange an interview with the Examiner and her supervisor to discuss the Formal Drawings. However, due to the Examiner's workload, Applicant's undersigned representative has not been able to schedule an interview as of today's date. Applicant's undersigned representative believes that a short interview would resolve the Examiner's objection to the drawings, and respectfully requests that the Examiner contact the Applicant's undersigned representative as soon as possible to schedule an interview.

2. Claims 1-15 and 17-30 stand rejected under 35 U.S.C. § 112, second paragraph as allegedly being indefinite. The Examiner alleges that claims 1-15 and 17-30 allegedly improperly embrace or overlap two different statutory classes of invention. Applicant respectfully traverses the rejection of claims 1-15 and 17-30 for at least the reasons set forth below.

Applicant herein amends claims 1, 2, 4, 5, 7-11, 13, 17 and 19 to replace the term "provided" with the term "disposed" in order to clarify that claims 1-15 and 17-30 are apparatus claims. Also, Applicant herein amends claims 1 and 17 to clarify the structural relationships between the recited elements in claims 1 and 17. The amendments to claims 1, 4, 5, 7-11, 13, 17 and 19 were not amended for reasons of patentability, and Applicant does not believe that the claim amendments narrow the literal scope of the claims. Although Applicant has amended these recitations for the reasons discussed above, Applicant submits that these particular recitations of claim 1 were sufficiently clear to one of skill in the art.

The Examiner alleges that, in claim 1, it is not clear what are "shallow trench isolating regions having a first depth, and provided in surface portions of said semiconductor substrate for defining active areas therebetween."

Referring to Figure 5 of the instant application, as one example of an embodiment of the invention, it is plainly evident that shallow trench isolating regions 13/16 are disposed inside heavily doped n-type region 15, and the shallow trench isolating regions 13/16 penetrate to the p-type well 12. Active areas, e.g., the heavily doped n-type source/drain regions 17a/17b, are disposed in the p-type well 12, and are positioned between the shallow trench isolating regions 13/16. *See, e.g.*, Fig. 5 and page 10, lines 4-10 of the instant application.

The Examiner alleges that, in claim 1, it is not clear what is "a circuit component of an integrated circuit provided in one of said active areas, and connected between said terminal and a first source of constant voltage."

With respect to the circuit component, referring to Figure 5 of the instant application, a terminal 1 is connected to an active area 17a, and the other active area 17b is coupled to a source of constant voltage. In Figure 5, as one example of an embodiment of the invention, this source of constant voltage is a ground potential. *See* Fig. 5 and page 10, line 23 to page 11, line 4 of the instant application. As one example of an embodiment of the invention, the circuit component is a field effect transistor 3 disposed over the active areas 17a/17b. *See* Fig. 5, page 9, lines 7-9 and page 11, lines 4-7.

Thus, Applicant believes that claims 1-15 and 17-30 are in condition for allowance, and request that the § 112, second paragraph rejection be withdrawn.

3. Claims 17-30 stand rejected under 35 U.S.C. § 101 as embracing two different statutory classes of invention.

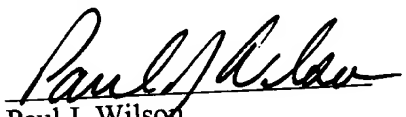
As noted above, Applicant herein amends claims 17 and 19 to replace the term "provided" with the term "disposed" in order to clarify that claims 17 and 19 are apparatus claims. The amendments to claims 17 and 19 were not amended for reasons of patentability, and Applicant does not believe that the claim amendments narrow the literal scope of the claims. Although Applicant has amended these recitations for the reasons discussed above, Applicant submits that these particular recitations of claims 17 and 19 were sufficiently clear to one of skill in the art. Applicant requests that the Examiner withdraw the § 101 rejection.

With respect to the Examiner's statement that a drawing that depicts claim 17 is required, please see the discussion above with respect to Figure 5 of the Formal Drawings. Figure 5, as described in the instant specification, adequately describes the subject matter recited in claim 17, and the Examiner has provided no substantive reasoning as to why the Formal Drawings do not support the claims. *See In re Zurko*, 258 F.3d 1379, 1386 (Fed. Cir. 2001).

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

The claims are amended as follows:

1. (*Twice Amended*) A semiconductor [integrated circuit] device [provided on a semiconductor substrate of one conductivity type,] comprising:

a semiconductor substrate of one conductivity type;

shallow trench isolating regions having a first depth, and disposed [provided] in surface portions of said semiconductor substrate and [for] defining active areas therebetween;

a terminal connected to one of said active areas [provided on said semiconductor substrate];

a first source of constant voltage connected to another of said active areas;

a circuit component [of an integrated circuit provided in one of said active areas, and] connected between said terminal and said [a] first source of constant voltage; and

a protection circuit disposed adjacent to [provided in] at least said one of said active areas, and comprising:

a first impurity region of said one conductivity type disposed adjacent to [provided under] said at least one of said active areas, wherein said first impurity region is a base region of a bipolar transistor,

a second impurity region of a second [the other] conductivity type opposite to said one conductivity type disposed adjacent to [provided in a surface portion of] said first impurity

region, connected to said terminal, wherein said second impurity region is one of an emitter region or [and] a collector region of said bipolar transistor; and

a third impurity region of said other conductivity type connected to said first source of constant voltage, [provided in another surface portion of said semiconductor substrate,] wherein said third impurity region is the other of said emitter region or [and] said collector region of said bipolar transistor.

2. (*Twice Amended*) The semiconductor [integrated circuit] device as set forth in claim 1, wherein said third impurity region further comprises:

a first impurity sub-region disposed [provided] in a surface portion of another active area adjacent to said one of said active areas; and

a second impurity sub-region contiguous to a bottom surface of said first impurity sub-region and extending in said first impurity region under said second impurity region.

3. (*Twice Amended*) The semiconductor [integrated circuit] device as set forth in claim 2, wherein said first impurity sub-region comprises:

a first portion contiguous to said second impurity sub-region; and

a second portion heavier in dopant concentration than said first portion and connected to said first source of constant voltage.

4. (*Twice Amended*) The semiconductor [integrated circuit] device as set forth in claim 2, wherein said circuit component is a field effect transistor comprising source and drain regions of said other conductivity type disposed [provided] in said one of said active areas, and one of said source and drain regions is said second impurity region.

5. (*Twice Amended*) The semiconductor [integrated circuit] device as set forth in claim 1, wherein said third impurity region comprises:

a first impurity sub-region disposed [provided] in another surface portion of said first impurity region spaced from said second impurity region; and

a second impurity sub-region contiguous to a bottom surface of said first impurity sub-region and extending in said first impurity region under said second impurity region.

6. (*Twice Amended*) The semiconductor [integrated circuit] device as set forth in claim 5, wherein said first impurity sub-region comprises:

a first portion contiguous to said second impurity sub-region; and

a second portion heavier in dopant concentration than said first portion and connected to said first source of constant voltage.

7. (*Twice Amended*) The semiconductor [integrated circuit] device as set forth in claim 5, wherein said circuit component is a field effect transistor comprising source and drain regions disposed [of said other conductivity type provided] in said one of said active areas, wherein one of

said source and drain regions is said second impurity region, and the other of said source and drain regions is said first impurity sub-region.

8. (*Twice Amended*) The semiconductor [integrated circuit] device as set forth in claim 1, wherein said third impurity region is disposed [provided] in another active area adjacent to said one of said active areas and having a second depth greater than said first depth.

9. (*Twice Amended*) The semiconductor [integrated circuit] device as set forth in claim 8, wherein said circuit component is a field effect transistor comprising source and drain regions disposed [of said other conductivity type provided] in said one of said active areas, and one of said source and drain regions is said second impurity region.

10. (*Twice Amended*) The semiconductor [integrated circuit] device as set forth in claim 1, wherein said third impurity region is disposed [provided] in another surface portion of said first impurity region and deeper than said second impurity region.

11. (*Twice Amended*) The semiconductor [integrated circuit] device as set forth in claim 10, wherein said circuit component is a field effect transistor comprising source and drain regions disposed [of said other conductivity type provided] in said one of said active areas, one of said source and drain regions is said second impurity region, and the other of said source and drain region is a part of said third impurity region.

12. (*Twice Amended*) The semiconductor [integrated circuit] device as set forth in claim 1, wherein said third impurity region extends in said first impurity region under said second impurity region.

13. (*Twice Amended*) The semiconductor [integrated circuit] device as set forth in claim 10, wherein said circuit component is a field effect transistor comprising source and drain regions disposed [of said other conductivity type provided] in said one of said active areas, and one of said source and drain regions is said second impurity region.

14. (*Twice Amended*) The semiconductor [integrated circuit] device as set forth in claim 1, wherein said terminal is a signal output terminal, and said circuit component is an output transistor.

15. (*Twice Amended*) The semiconductor [integrated circuit] device as set forth in claim 1, wherein said terminal is a signal input and output terminal, and said circuit component is an output transistor comprising a portion of an input and output circuit connected to said terminal.

17. (*Amended*) A semiconductor [integrated circuit] device [provided on a semiconductor substrate of a first conductivity type,] comprising:

a semiconductor substrate of a first conductivity type;

a plurality of active areas disposed [provided] in a portion of said semiconductor substrate;

at least one shallow trench isolation region disposed between said active areas;

a terminal connected to one of said active areas;

a first source of constant voltage connected to another of said active areas;

a circuit component connected between said terminal and said [a] first source of constant voltage; and

a protection circuit disposed adjacent to [provided in] at least said one of said active areas, said protection circuit comprising:

a first impurity region of said first conductivity type disposed adjacent to [provided under] at least one of said active areas and serving as a base region of a bipolar transistor,

a second impurity region of a second conductivity type opposite to said first conductivity type disposed [provided] in said active area connected to said terminal, and serving as one of an emitter region or [and] a collector region of said bipolar transistor; and

a third impurity region of said second conductivity type connected to said first source of constant voltage, disposed [provided] in another portion of said semiconductor substrate and serving as the other of said emitter region or [and] said collector region of said bipolar transistor.

18. (*Amended*) The semiconductor [integrated circuit] device as set forth in claim 17, wherein said circuit component is a field effect transistor.

19. (*Amended*) The semiconductor [integrated circuit] device as set forth in claim 17, wherein said third impurity region further comprises:

a first impurity sub-region disposed [provided] in a surface portion of an active area adjacent to said at least one shallow trench isolation region; and

a second impurity sub-region contiguous to a bottom surface of said first impurity sub-region.

20. (*Amended*) The semiconductor [integrated circuit] device as set forth in claim 18, wherein said first impurity sub-region comprises a first portion contiguous to said second impurity sub-region.

21. (*Amended*) The semiconductor [integrated circuit] device as set forth in claim 20, wherein said first impurity sub-region further comprises a second portion heavier in dopant concentration than said first portion and connected to said first source of constant voltage.

22. (*Amended*) The semiconductor [integrated circuit] device as set forth in claim 17, wherein said at least one shallow trench isolation region has a first depth and said third impurity region has a second depth greater than said first depth.

23. (*Amended*) The semiconductor [integrated circuit] device as set forth in claim 17, wherein the depth of said third impurity region is deeper than the depth of said second impurity region.

24. (*Amended*) The semiconductor [integrated circuit] device as set forth in claim 17, wherein said third impurity region extends into said first impurity region under said second impurity region.

25. (*Amended*) The semiconductor [integrated circuit] device as set forth in claim 17, wherein an upper surface of said third impurity region is contiguous with a bottom surface of said first impurity region.

26. (*Amended*) The semiconductor [integrated circuit] device as set forth in claim 17, wherein said first impurity region is a p-type impurity region.

27. (*Amended*) The semiconductor [integrated circuit] device as set forth in claim 17, wherein said second impurity region is a n-type impurity region.

28. (*Amended*) The semiconductor [integrated circuit] device as set forth in claim 17, wherein said third impurity region is a n-type impurity region.

29. (*Amended*) The semiconductor [integrated circuit] device as set forth in claim 17, wherein said terminal is a signal output terminal and said circuit component is an output transistor.

30. (*Amended*) The semiconductor [integrated circuit] device as set forth in claim 17, wherein said terminal is a signal input and output terminal, and said circuit component is an output transistor comprising a portion of an input and output circuit connected to said terminal.